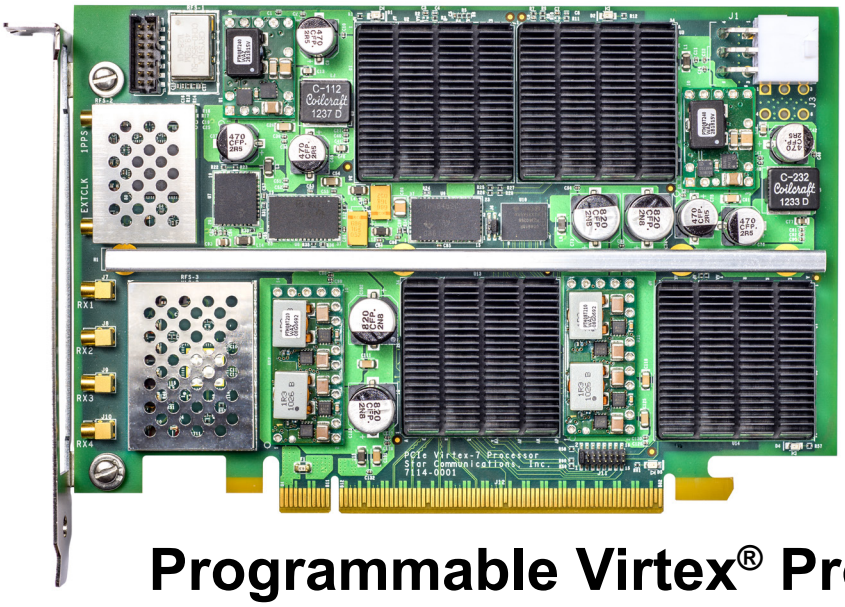
Star Communications, Inc.

PVP-7xx Receiver



Introducing the world's most powerful FPGA digital receivers...

Programmable Virtex® Processor Card

The PVP-7xx family combines a multi-channel digital receiver with one or more FPGA processing elements, on a standard PCI Express® card. A single card can execute over $6x10^{12}$ multiply-and-accumulate operations per second, making it the most powerful signal processing card available today!

When installed in a customer's host system, such as a rack-mount server or other PCIe host, a PVP-7xx provides a complete IF-to-DMA path for receiving wireless signals, processing them in an FPGA, and sending results to host CPU(s) via PCI Express.

External equipment mixes radio signals down to an appropriate intermediate frequency (IF), and after filtering, inputs the signals to the PVP card. The IF design allows a single card to be used for satellite, cellular, microwave, H/U/VHF, radar, or any combination.

The PVP-7xx has up to four input channels, which are sampled to 12-bit resolution using a programmable sampling clock between 100 and 250 megasamples per second. Onboard sample clock generation is provided, or customers may supply their own clock or reference signal via an external input port.

All channels of digitized data are routed to each FPGA. Each FPGA is a Virtex®-7 XC7VX485T component, manufactured by Xilinx, Inc. A VX485 contains 2800 DSP48, 2060 BRAM of 18Kbits, and 75900 slices, each having four 6-input LUT and eight FF. This provides an ideal mix for signal processing applications.

Using a simple application programming interface (API), customers can access the sampled radio signals, and write VHDL or Verilog code to process the signals. Results can be forwarded to host CPUs using the direct memory access API. Each FPGA contains 1024 DMA read and write engines. On the host side, the job of interfacing to each FPGA is handled by a Linux device driver supplied with the card. Convenient access to the device drivers is provided by a set of C routines called the application API.

PCI EXPRESS® VIRTEX 7

Ordering Information

PVP-7xx

- Number of FPGA's (1-4)
- Number of Digital Receivers (0-4)

Made in the U.S.A.

Digital Receivers

Number of Receivers	0, 1, 2, 3, or 4
Resolution	12 bits
Sampling Frequency	100 to 250 MHz (programmable)
Receiver Bandwidth	10 to 300 MHz
Impedance	50 Ω
Connector Type	MMCX jack (e.g. Amphenol 908-24100)

Clocking

Sample Rate	Programmable (sub-Hz resolution)
Sample Rate Range	100 to 250 Msps
Internal Reference Clock	±2.5 ppm frequency stability
External Clock	50 Ω, -10 to +10 dBm, 10 to 250 MHz
External Trigger	50 Ω or TTL/CMOS, 1.8 to 5.0 Volts
External Connectors	MMCX jack (e.g. Amphenol 908-24100)

Processing

Operating System	Red Hat Enterprise Linux (RHEL) release 6.4
Firmware API	VHDL-93
Linux Device Driver	C, using the GNU compiler (gcc-4.4.6-3.el6.x86 64)
Software API	C, using the GNU compiler (gcc-4.4.6-3.el6.x86 64)
FPGA Development Tool	Xilinx ISE™ version 14.5
Development Interfaces	Downloadable Flash, Xilinx Platform Cable USB (Model DLC9G)
Number of FPGAs	1, 2, 3, or 4 (Xilinx XC7VX485T)

Host Interface

Interface Type	PCI Express version 1.1 (Gen1) or 2.1 (Gen2)
Signaling Rate	2.5 or 5.0 Gbit/sec per lane
Number of Active Lanes	1 to 8 lanes per card, 1 to 2 lanes per FPGA
PCIe Connector	x16 standard PCIe card edge connector
Configuration Registers	PCI™ Type 0 (Endpoint) Configuration Space
Data Transfer	DMA (1024 read/write engines)

Electro-Mechanical

Card Size (exact)	PCIe standard height, half length, x16 add-in card
Card Size (approx.)	6.6 by 4.4 by 0.8 inches
Power Consumption	Configuration dependent (50 to 125 Watts)
Auxiliary Power Connector	0 or 1, PEG-6 standard PCIe connector (e.g. Molex 39-30-0060)
Auxiliary Connector Location	Factory option (90° rear or top facing, vertical mount, or floating)

With the purchase of a PVP-7xx card and software development kit license, customers receive the following items: one PVP-7xx card with installed front panel, coaxial cables for MMCX-to-SMA adaption, an FPGA software development kit compatible with VHDL or Verilog, and a C/C++ software development kit including Linux device drivers and API routines for use on the host system.